Kaiwei Tu

Email: tukaiwei@outlook.com, Github: https://github.com/Kaiweitu

Education

University of Wisconsin - Madison **Madison, WI**
Ph.D. candidate in Computer Science *Sept 2019 - Present*
Advisor: Prof. Remzi H. Arpaci-Dusseau and Prof. Andrea C. Arpaci-Dusseau

University of Michigan **Ann Arbor, MI**
Bachelor of Science in Engineering major in Computer Science, Summa Cum Laude (highest distinction) *April 2019*

Shanghai Jiao Tong University **Shanghai, China**
Bachelor of Science in Electrical and Computer Engineering *August 2017*

Research Experience

The ADvanced Systems Laboratory (ADSL) **Ann Arbor, MI**
Research Assistant *April 2021 - present*

- My current research focus is redesigning existing software technology over emerging storage devices. My ongoing project is rethinking caching over a modern storage hierarchy composed of new storage devices such as persistent memory.
- **Orthus** is a research project published on **FAST'21** which proposes a new caching mechanism named Non-Hierarchy Caching that can dynamically offload the saturated caching device if necessary. Specifically, I implement serval state-of-art caching strategies in Intel's open-source caching framework, Open CAS Linux, to compare against NHC, which shows that NHC outperforms previous approaches in a broader range of workloads, especially dynamic workloads.
- **NyxCache** is a research project published on **FAST'22** that proposes a flexible and efficient caching framework for multi-tenancy cache over PM. One of my primary contributions is implementing the Nyx-controller, a significant component of enforcing different sharing policies upon a multi-tenant cache. In addition, I conducted experiments to show that NyxCache could correctly enforce policy such as quality-of-service, proportional sharing, and fair slowdown while the traditional DRAM-based method couldn't.

Work Experience

Google **Sunnyvale, CA**
Research Intern *May 2022 - Aug 2022*

- The project I am working on is about evaluating and designing node-level memory bandwidth QoS mechanism on AMD machines in the cluster. Specifically, I systematically evaluate and compare four memory bandwidth regulation mechanisms and purpose a hybrid policy that combing cpu jailing and resctrl that could achieve efficient memory bandwidth regulation at scale.

University of Wisconsin - Madison **Madison, WI**
Introduction to OS, Teaching Assistant *Jan 2020 - April 2020, Jan 2021 - April 2021*

- Created hand-on xv6-based kernel projects relating to virtual memory and file system checkers.
- Led weekly lab section and office hours for lecture content and project-related questions.

Citrix System **Fort Lauderdale, FL**
Software Development Engineering Intern *April 2018 – August 2018*

- Enhanced a provisioning service that can automatically deploy Citrix VM on the cloud.
- Led, designed and developed a new interface for users to check provisioning information by creating corresponding RESTful API, utilizing BootStrap as the front-end frame and Spring Boot and MySQL as the back-end.

Publications

[1] Kan Wu, **Kaiwei Tu**, Yuvraj Patel, Rathijit Sen, Kwanghyun Park, Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau. NyxCache: Flexible and Efficient Multi-tenant Persistent Memory Caching. In *Proceedings of the 20th USENIX Conference on File and Storage Technologies* (FAST '22), February 2022.

[2] Kan Wu, Zhihan Guo, Guanzhou Hu, **Kaiwei Tu**, Ramnatthan Alagappan, Rathijit Sen, Kwanghyun Park, Andrea C. Arpaci-Dusseau, and Remzi H. Arpaci-Dusseau. The Storage Hierarchy is Not a Hierarchy: Optimizing Caching on Modern Storage Devices with Orthus. In *Proceedings of the 19th USENIX Conference on File and Storage Technologies* (FAST '21), Virtual, February 2021.

Awards & Grants

- USENIX Student Grant: FAST'22
- James B. Angell Scholar: achieve an "A" record for two or more consecutive terms
- Dean's List: 2017 Fall, 2018 Spring, 2018 Fall, 2019 Spring