Kaiwei Tu

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Madison, WI
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Education

University of Wisconsin–Madison **Madison, WI**
Ph.D. Candidate in Computer Science *2021–Present*
Advisor: Prof. Remzi H. Arpaci-Dusseau and Prof. Andrea C. Arpaci-Dusseau

University of Wisconsin–Madison **Madison, WI**
M.S. in Computer Science *2019–2021*

University of Michigan **Ann Arbor, MI**
B.S. in Engineering, Computer Science (Summa Cum Laude) *2015–2019*

Shanghai Jiao Tong University **Shanghai, China**
B.S. in Electrical and Computer Engineering *2013–2017*

Research Interests

Storage systems, Caching and tiering schemes, Operating systems, AI and system Co-design.

Publications

[1]: **Kaiwei Tu**, Kan Wu, Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau. "Getting the MOST out of your Storage Hierarchy with Mirror-Optimized Storage Tiering." *FAST '26*, To appear.

[2]: Kan Wu, **Kaiwei Tu**, Yuvraj Patel, Rathijit Sen, Kwanghyun Park, Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau. "NyxCache: Flexible and Efficient Multi-tenant Persistent Memory Caching." *USENIX FAST '22*, February 2022.

[3]: Kan Wu, Zhihan Guo, Guanzhou Hu, **Kaiwei Tu**, Ramnatthan Alagappan, Rathijit Sen, Kwanghyun Park, Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau. "The Storage Hierarchy is Not a Hierarchy: Optimizing Caching on Modern Storage Devices with Orthus." *USENIX FAST '21*, February 2021.

Research Experience

The ADSL (Advanced Systems Laboratory), UW–Madison **Madison, WI**
Research Assistant *Apr 2021–Present*

- MOST (FAST '26): Developing a mirror-optimized tiering scheme for heterogeneous storage hierarchies.
- NyxCache (FAST '22): Designed and implemented the Nyx-controller for multi-tenant persistent-memory caching; conducted QoS, proportional sharing, and fair slowdown policy evaluations.
- Orthus (FAST '21): Implemented Non-Hierarchy Caching (NHC) in Intel's Open CAS Linux kernel module and evaluated its performance under dynamic workloads.

Professional Experience

Meta **Menlo Park, CA**
Software Engineering Intern *May 2025–Aug 2025*

- Building an AI workload benchmark for CPU on the AI & System Co-design Compute and Storage team.

Google **Sunnyvale, CA**

Research Intern *May 2022–Aug 2022*

- Evaluated memory bandwidth regulation mechanisms on AMD machines across Google's fleet; proposed a hybrid CPU-jailing and resctrl policy improving regulation efficiency.

Citrix Systems **Fort Lauderdale, FL**

Software Development Engineer Intern *Apr 2018–Aug 2018*

- Enhanced cloud VM provisioning service; led development of a RESTful API and UI for deployment monitoring.

Teaching Experience

University of Wisconsin–Madison **Madison, WI**

Teaching Assistant, Advanced Operating Systems *Fall 2023*

- Led discussion sections, designed problem sets, and managed grading for a graduate-level OS course.

University of Wisconsin–Madison **Madison, WI**

Teaching Assistant, Introduction to Computer Systems *Spring 2023*

- Held office hours, assisted students in laboratory exercises, and provided exam review sessions.

Honors & Awards

2022: USENIX Student Grant, FAST '22

2019: James B. Angell Scholar

2018: EECS Scholars

2017–2019: Dean's List; University Honors

Academic Services

2025: Eurosys'26 Shadow PC

References

Advisors: Prof. Remzi H. Arpaci-Dusseau (remzi@cs.wisc.edu) and Prof. Andrea C. Arpaci-Dusseau (dusseau@cs.wisc.edu)